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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,902	08/11/2000	Kozo Harada	50090-234	8376

7590 10/23/2003

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/635,902	HARADA ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20 - 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20 - 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 4, 2003 has been entered. An action on the RCE follows.

2. Applicant's amendment filed on August 4, 2003 has been received and entered in the case.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

Regarding claim 21, the drawings fail to show a combined structure that contains the following limitations in claims 20 and 21 a "second electrode" and an "insulating layer" on the same surface of the semiconductor chip must be shown or the feature(s) canceled from the

claim(s). No new matter should be entered. The drawings in the instant invention do not show both limitations in one figure.

Regarding claim 25, the drawings fail to show a combined structure of claims 22 and 25 "conductive line patterns" formed on the both surfaces of the lower semiconductor chip must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 21 and 25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 21, the specification fails to disclose the combined structure of claims 20 and 21 that both elements a "second electrode" and an "insulating layer" are formed on the same surface of the semiconductor chip.

In claim 25, the specification fails to disclose the combined structure of claims 22 and 25 that "conductive line patterns" are formed on both surfaces of the lower of the semiconductor chip.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 20 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Oda.

Regarding claim 20, Oda discloses in FIG. 1 a semiconductor device comprising:

- a semiconductor chip (1);
- at least a first electrode (2) formed on a first major surface of the semiconductor chip;

- at least a second electrode (5) formed on a second major surface of the semiconductor chip opposite to the first major surface; and
- at least a conductive member (4) connecting the first electrode to the second electrode and covering a side surface of the semiconductor chip.

Regarding claim 23, Oda discloses in FIG. 1 at least two semiconductor devices as defined in claim 20, wherein

- the at least two semiconductor devices are stacked on each other; and
- Since Oda discloses in Fig. 1 an electrical connection between the conductive members of lower and upper one of the semiconductor devices, semiconductor device of Oda are electrically connected. Therefore, Oda discloses the following limitation "a conductive member of a lower one of the semiconductor devices is connected to a conductive member of an upper one of the semiconductor devices"

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda in view of Hsuan et al.

Regarding claim 21, Oda discloses the claimed invention except for the second major surface is formed of an insulating layer. However, Hsuan et al. teaches in Fig. 2I and column 3, lines 11 ~ 13 a second major surface being formed of an insulating layer (48d). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Oda by using the insulating layer as taught by Hsuan et al. The one of ordinary skill in the art would have been motivated to modify Oda in the manner described above for at least the purpose of protecting the pad.

Regarding claim 24, Oda discloses in Fig. 1 at least two semiconductor devices as defined in claim 21, wherein

- the at least two semiconductor devices are stacked on each other, and
- a conductive member of a lower one of the semiconductor devices is connected to a conductive member of an upper one of the semiconductor devices.

11. Claims 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda in view of Eide.

Regarding claim 22, Oda discloses the claimed invention except for a conductive line pattern extending from the second electrode. However, Eide teaches in Fig. 3, Fig. 6a and Fig. 7 a conductive line pattern (7) extending from a second electrode (5, at the bottom of the element 8). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Oda by using the conductive line pattern as taught by Eide. The one of ordinary skill in the art would have been motivated to modify Oda in the manner

described above for at least the purpose of providing the ability to transpose connections to different ball grid contact positions (column 2, lines 28 ~ 34).

Regarding claim 25, Oda discloses at least two semiconductor devices as defined in claim 22, wherein the at least two semiconductor devices are stacked on each other. However, Oda does not disclose a conductive line pattern extending from a first electrode on a first major surface of a lower one of the semiconductor devices is connected via a bump to a conductive line pattern extending from a second electrode on a second major surface of an upper one of the semiconductor devices. Eide teaches in Fig. 3, Fig. 6a and Fig. 7 a conductive line pattern (7) extending from a first electrode (5, at the top) on a first major surface of a lower one of the semiconductor devices (the lowest device in Fig. 7) being connected via a bump (14) to a conductive line pattern (7) extending from a second electrode (5, at the bottom) on a second major surface of an upper one of the semiconductor devices (the second device from the bottom). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Oda by using the conductive line pattern on the first and second major surfaces as taught by Eide. The one of ordinary skill in the art would have been motivated to modify Oda in the manner described above for at least the purpose of providing the ability to transpose connections to different ball grid contact positions (column 2, lines 28 ~ 34).

12. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oda and Hsuan et al. as applied to claims 20 and 21 above, and further in view of Pierson et al.

Regarding claim 26, Oda and Hsuan et al. disclose the claimed invention except for a packaging board having a conductive pattern on a major surface thereof and a plurality of

semiconductor devices as defined in claim 21, placed vertically on the major surface of the packing board, wherein each of the conductive member covering the side surface of the semiconductor chip is connected to the conductive pattern on the major surface of the packaging board. However, Pierson et al. teaches in Fig. 1A a packaging board (11, at the bottom) having a conductive pattern (15) on a major surface thereof and a plurality of semiconductor devices (11 and 21) as defined in claim 21, placed vertically on the major surface of the packing board, wherein each of the conductive member covering the side surface of the semiconductor chip is connected (14) to the conductive pattern on the major surface of the packaging board. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Oda by using the packaging board as taught by Pierson et al. The one of ordinary skill in the art would have been motivated to further modify Oda in the manner described above for at least the purpose of providing a structure for facilitating edge mounting of chips on a substrate or another chip (column 3, lines 63 ~ 65).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
10/16/03 9:06:55 PM

GEORGE ECKERT
PRIMARY EXAMINER